EV-129
AAT1230 EVAL:
18V/10V 100mA Boost Converter

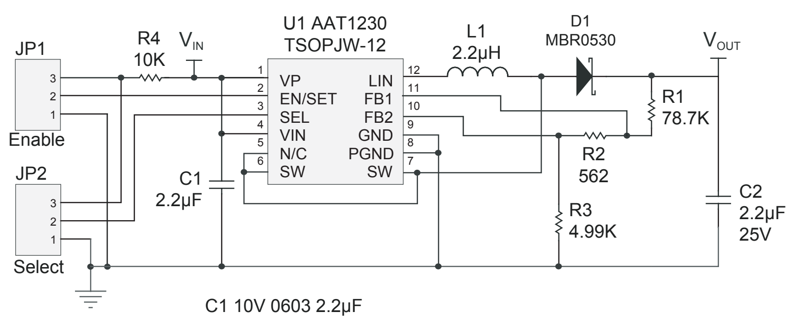
Introduction

The AAT1230 evaluation board provides a platform for test and evaluation of the AAT1230 switching boost regulator. The evaluation board demonstrates the suggested size and placement of external components to achieve output voltages from 10V to 18V and up to 100mA output load. The external components are selected for small size to suit portable applications, while the layout has been optimized to achieve high efficiency and low output noise with the TSOPJW-12 package. The AAT1230 operates across an input voltage range from 2.7V to 5.5V.

The AAT1230 evaluation board provides a single 18V output or 10V output at 100mA maximum output current. The desired output is determined by the logic level of the SEL pin, which is set by the JP2 jumper setting. Connecting SEL (JP2) to logic high (V_{IN}) sets the output voltage to 18V while logic low (GND) sets the output voltage to 10V.

This document provides details on the operation and testing of the AAT1230 evaluation board. Modification of the resistor divider network (R1, R2, R3) allows outputs from 10V to 18V and up to 100mA.

Operating Specifications, Schematic, and BOM



C1 10V 0603 2.2μF
C2 25V 0805 2.2μF
D1 30V 0.5A MBR0530T1 SOD-123
L1 2.2μH SD3814-2R2
R1 78.7k 0603
R2 562 0603
R3 4.99k 0603
R4 10k 0603

Figure 1: AAT1230 Evaluation Board Schematic (AAT1230-DB2).

Specification	Test Conditions	Min	Typ	Max	Units
Input Voltage		2.7		5.5	V
Output Error Voltage	V_{OUT} = 10V to 18V; 1% Tolerance R1, R2, R3	-4.0		4.0	%
Output Voltage	EN = V_{IN} (JP1), SEL = V_{IN} (JP2)		18.0		V
	EN = V_{IN} (JP1); SEL = GND (JP2)		10.0		
	EN = S^2CWire™[1]; SEL = GND (JP2)	10.0		18.0[2]	
Output Current	V_{IN} = 2.7V to 5.5V	0		100	mA

Table 1: AAT1230 Evaluation Board Operating Specifications.

1 Contact an AnalogicTech sales representative for information on Simple Serial Control™ (S^2Cwire) programming options.
2 Maximum nominal output voltage should be limited to 18V to avoid damaging the AAT1230 device.

Test Equipment

1. Unit under test (UUT) is the AAT1230 Evaluation Board.
2. 6.0V (minimum) 2.0A laboratory input power supply: HP33401A or equivalent.
3. DC 0A to 0.5A electronic load capable of operation up to 20V: Keithley 2400 or equivalent. When using the Keithley 2400, set the meter to operate in voltage source mode and set the load current by varying the current compliance (maximum current) of the meter.
4. Two (2) DC voltmeters: Fluke 189 or equivalent; set to DCV setting.
5. Oscilloscope: Tektronix TS744A or equivalent; Tektronix P6139 oscilloscope probes or equivalent.
6. Miscellaneous test leads (banana plug to clip lead type is recommended). Conductor thickness is not important for low current levels of UUT.
7. Aluminum electrolytic or tantalum input decoupling capacitor: 10µF to 120µF, ≥ 10V.
8. Optional S²Cwire interface for 16-level dynamic voltage programmability. Contact an AnalogicTech sales representative for information on S²Cwire programming options.

Set-Up

1. Configure the specified test equipment, as shown in Figure 2. JP1, JP2, and S²Cwire options are shown.
2. An additional 10µF to 120µF input capacitor may be required to decouple the input power supply and maintain stable operation. Solder to input pins.
3. Input power supply with remote sense is optional (not shown in Figure 2). This simplifies the test procedure and maintains high accuracy of the input voltage across the load range. Connect remote sense from input power source remote sense terminals to VIN and GND terminals on the UUT.

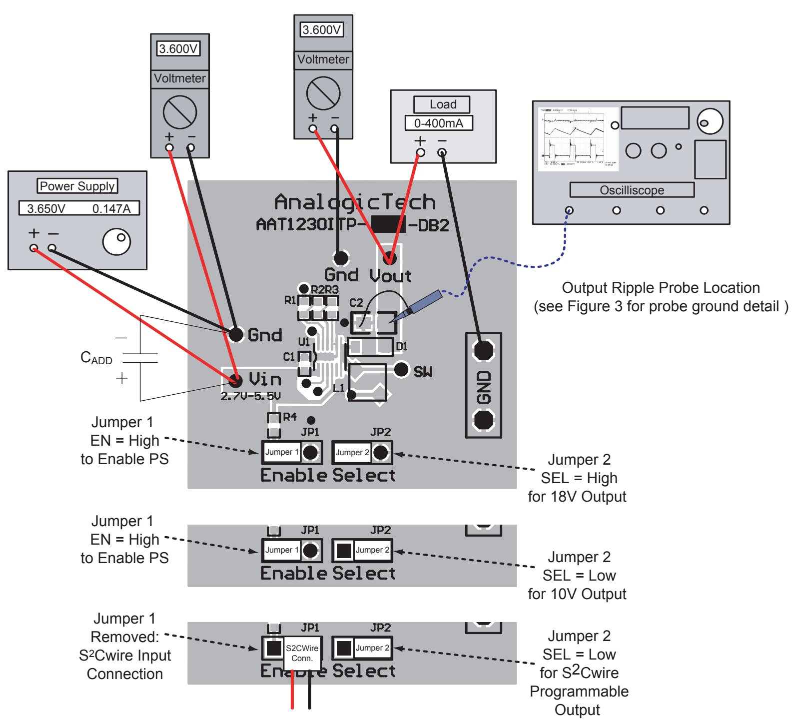


Figure 2: AAT1230 Evaluation Board Connection Diagram and JP1, JP2 Settings.

Test

Load and Line Regulation

1. Enable the UUT jumper JP1 to the ON position. Select JP2 position based on desired DC output voltage (10V or 18V), as shown in Figure 2.
2. Turn on the input power supply and set to desired input voltage based on the DC voltmeter.
3. Vary the output load from 0A to 100mA and vary the input voltage from 2.7V to 5.5V while monitoring the output voltage.

Enable Turn-On and Turn-Off

1. With input voltage applied, remove JP1 and reinsert in the OFF position.
2. The output voltage should decay to zero.
3. Remove JP1 and reinsert in the ON position. The output voltage should recover to its initial DC value.

Output Ripple Measurement

1. Configure oscilloscope CH1 for output ripple measurement. Plug probe into CH1, as shown in Figure 2.
   a. AC coupling, 100mV/div.
   b. BW < 100MHz to limit high frequency probe pick-up.
2. Configure oscilloscope to trigger on CH1 rising or falling edge.
3. Turn on input power supply. Set input voltage between 2.7V and 5.5V and adjust output load from 0mA to 100mA, as desired. It should be noted that light load measurements (<20mA) may be affected by electronic load characteristics. As an alternative, parallel arrangement of 1/4W carbon film resistor(s) can be used.
4. To minimize high frequency noise pick-up due to PCB parasitics and guarantee consistent results, CH1 output ripple should be measured directly across output capacitor C2, as shown in Figure 2. Probe tip contacting capacitor positive terminal. Probe ground consisting of a small bus wire wrapped around probe ground (see Figure 3). Probe GND contacting capacitor C2 return conductor for best results.

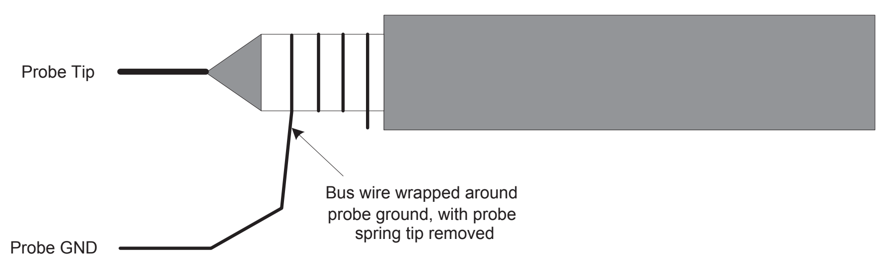


Figure 3: Oscilloscope Probe Set-Up for Output Ripple Measurement.

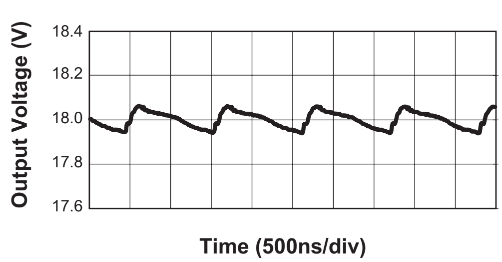


Figure 4: Typical Output Ripple: 18V @ 100mA; V_{IN} = 2.7V.

Output Voltage Setting

SEL Logic Pin Voltage Programming

The output voltage can be set to any voltage between 10V and 18V. Table 2 provides resistor combinations for common output voltages.

For specific output voltages not shown in Table 2, the following calculations can be utilized. Nearest 1% resistor value is recommended for optimum output voltage tolerance.

R3 = 4.99kΩ, 1%

$V_{OUT(1)} > V_{OUT(2)}$

Select nearest 1% R1, R2 value(s) from calculation:

$$X_{(2)} = \frac{V_{OUT(2)}}{0.6} - 1$$

$$X_{(1)} = \frac{V_{OUT(1)}}{1.2} - 1$$

$$R_1 = R_3 \cdot X_{(2)} \cdot \left(\frac{1 + X_{(2)}}{X_{(2)} + \frac{X_{(2)}}{X_{(1)}}}\right)$$

$$R_2 = R_1 \cdot X_{(2)} \cdot \left(\frac{\frac{X_{(2)}}{X_{(1)}} - 1}{1 + X_{(2)}}\right)$$

Verify $V_{OUT(1)}$, $V_{OUT(2)}$

$$V_{OUT(1)} = 1.2 \cdot \left(\frac{R_1}{R_2 + R_3} + 1\right)$$

$$V_{OUT(2)} = 0.6 \cdot \left(\frac{R_1 + R_2}{R_3} + 1\right)$$

$V_{OUT(1)}$ (SEL = High)	$V_{OUT(2)}$ (SEL = Low)	R3 = 4.99kΩ R1 (kΩ)	R2 (kΩ)
10.0V	–	36.5	0
12.0V	–	44.2	0
15.0V	–	57.6	0
16.0V	–	61.9	0
18.0V	–	69.8	0
–	10.0V	78.7	0
–	12.0V	95.3	0
–	15.0V	121	0
–	16.0V	127	0
–	18.0V	143	0
12.0V	10.0V	75	3.32
15.0V	10.0V	76.8	1.65
16.0V	10.0V	76.8	1.24
18.0V	10.0V	78.7	0.562
15.0V	12.0V	90.9	3.01
16.0V	12.0V	93.1	2.49
18.0V	12.0V	93.1	1.65
18.0V	15.0V	115	3.32

Table 2: SEL Pin Voltage Control Resistor Values.

Printed Circuit Board

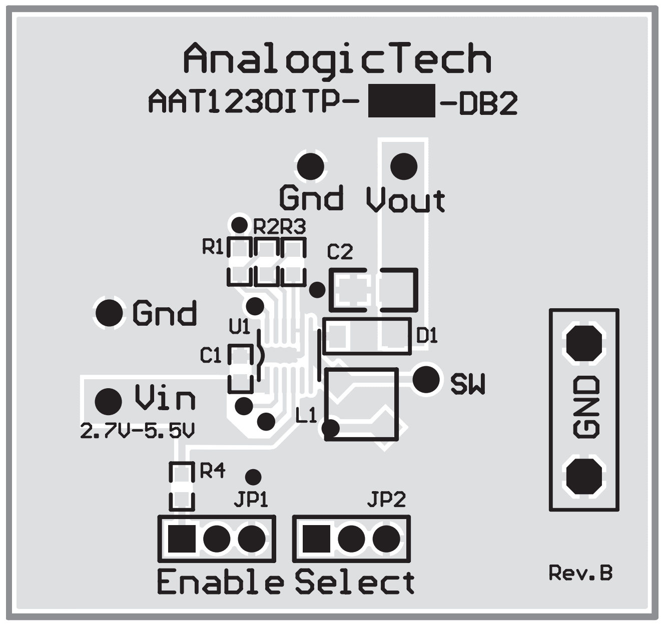


Figure 4: AAT1230 Evaluation Board Top Layer (not to scale).

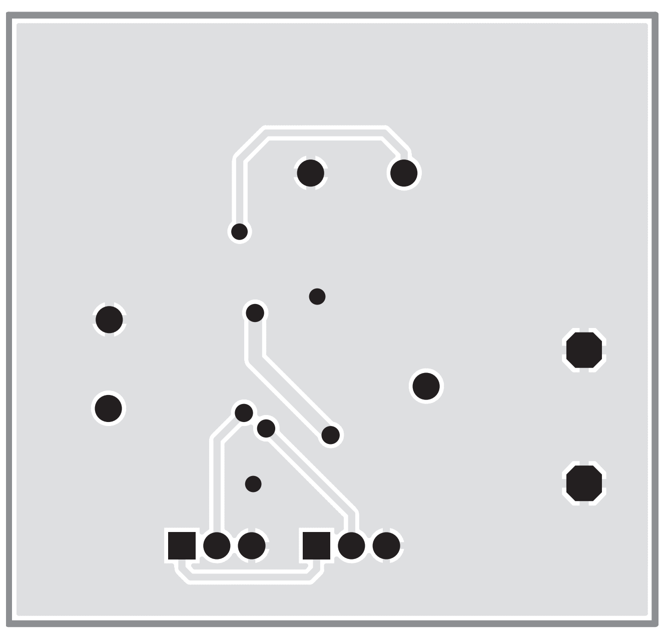


Figure 5: AAT1230 Evaluation Board Bottom Layer (not to scale)

Advanced Analogic Technologies, Inc.
830 E. Arques Avenue, Sunnyvale, CA 94085
Phone (408) 737-4600
Fax (408) 737-4611